ABSTRACT OF THE DISCLOSURE

It is an object to increase a speed of a CPU operation irrespective of an operation speed of a peripheral circuit and to prevent an increase in power consumption from being thereby caused. A clock generating circuit (10) generates two clocks having phases which are equal to each other, that is, a CPU clock (CLK_{CPU}) and a bus clock (CLK_{BUS}). A BIU (bus interface unit) (51) controls a code bus based on the CPU clock (CLK_{CPU}) and controls a peripheral bus based on the bus clock (CLK_{BUS}). The clock generating circuit (10) switches a frequency of each of the CPU clock (CLK_{CPU}) and the bus clock (CLK_{BUS}) depending on an operation mode of an MCU. For example, a speed of the CPU clock (CLK_{CPU}) is set to be higher than that of the bus clock (CLK_{BUS}) in order to carry out a high-speed operation of a CPU. Also in that case, the phases of both clocks are equal to each other. Consequently, the code bus and the peripheral bus in the BIU (51) can easily be controlled.